INFORMATION DISCLOSURE CITATION

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Docket Number (Optional)	Application Number
BUR920020023US1	10/063,142
Applicant(s)	
Timothy Lehner, et al.	
Filing Date	**Group Art Unit**
03/25/02	

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL	REF	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
JMP		5,481,484	01/02/96	Ogawa et al.			
		5,535,146	07/09/96	Huang et al.			
		5,652,716	07/29/97	Battersby et al.			
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	REF	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

JMP		Bina Ackalloor, Dinesh Gaitonde, "An Overview of Library Characterization in Semi-Custom Design" 5/97 IEEE 1998 Custom Integrated Circuits Conference, pp. 305-312
JMP		Jerry D. Hayes and Larry Wissel, "Behavioral Modeling for Timing, Noise, and Signal Integrity Analysis" IBM Microelectronics Division

EXAMINER	DATE CONSIDERED
Gregory Kessler	8/4/2005

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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JYP		6,080,201	06/27/00	Hojat, et al.			
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		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO

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JYP			Chandrakasan et al., "Design of High-Performance Microprocessor Circuits" ISBN 0-7803-6001-X, IEEE Order No. PC5836, Chapter 16.3 pp. 338-345
JYP			Jessica Qian, et al., "Modeling the 'Effective Capacitance' for the RC Interconnect of CMOS Gates" December 1994, Volume 13. No. 12, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems pp. 1526-1535

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	8/4/2005

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